PROGRAMME EDUCATIONAL OBJECTIVES (PEOs) :

I. To enrich students to excel in research leading to cutting edge technology in VLSI design and embedded systems and creating competent, innovative, and productive professionals in this field.
II. To provide students with a solid foundation in digital and computer architecture principles leading to VLSI design.
III. To understand the various applications and employ embedded systems to find solutions to them with good scientific and engineering knowledge so as to comprehend, analyze, design, and create novel products and solutions for the real life problems.
IV. To provide students with an academic environment aware of excellence, leadership, ethical conduct, positive attitude, societal responsibilities and the lifelong learning needed for a successful professional career.
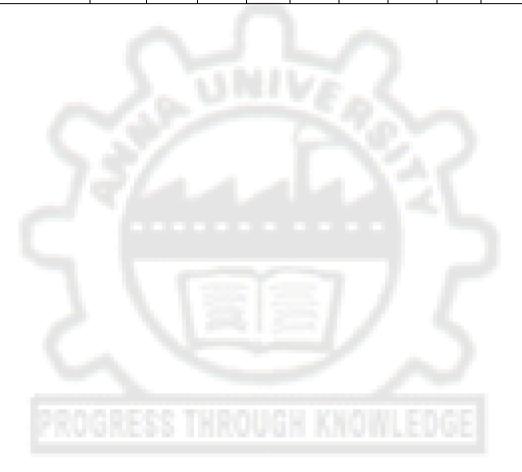V. To inculcate entrepreneurial skills in starting industries applying embedded system technologies.

PROGRAMME OUTCOMES (POs):
On successful completion of the programme,
1. Graduates will be able to apply the knowledge of computing, mathematics, science and electronic engineering for designing VLSI circuits.
2. Graduates will have an ability to identify, formulate, investigate and solve the issues related to the design of VLSI and embedded systems.
3. Graduates will have an ability to design and conduct experiments, perform analysis and interpret the problems of VLSI design and embedded systems.
4. Graduates will be able to demonstrate the design of an embedded system, component or process as per needs and specifications.
5. Graduates will demonstrate an ability to visualize and work on laboratory and multidisciplinary tasks.
6. Graduates will have the skills to use modern engineering tools, softwares and equipments to analyze problems.
7. Graduates will demonstrate knowledge of professional and ethical responsibilities.
8. Graduate will be able to communicate effectively in both verbal and written form.
9. Graduate will show the understanding of the impact of engineering solutions on the society and also will be aware of contemporary issues.
10. Graduate will develop confidence in self education and ability for lifelong learning.

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Programme Educational Objectives	Programme Outcomes									
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10
I	✓	✓	✓	✓	✓	✓		✓	✓	✓
II		✓	✓		✓	✓				
III				✓	✓	✓	✓			
IV		✓	✓				✓	✓	✓	✓
V		✓	✓	✓				✓	✓	✓

2

YEAR	SEM	SUBJECTS	PROGRAM EDUCATIONAL OBJECTIVES									
			PE1	PE2	PE3	PE4	PE5	PE6	PE7	PE8	PE9	PE10
First	I	Advanced Applied Mathematics	✓	✓			✓				✓	
		Digital Integrated Circuit Design		✓	✓	✓	✓	✓				
		Introduction to Embedded Controllers		✓		✓	✓	✓			✓	
		CMOS Analog IC Design		✓	✓		✓	✓				
		Design for Testability		✓	✓	✓	✓	✓	✓	✓		
		Elective-I										
		Analog & Digital System Design Lab			✓	✓	✓	✓	✓	✓		✓
	II	Real Time Embedded Systems		✓		✓	✓	✓			✓	
		VLSI Architectures for System Design		✓	✓	✓	✓	✓	✓		✓	✓
		Hardware-Software Co-design of Embedded system		✓	✓	✓	✓	✓	✓		✓	✓
		Low Power VLSI Design	✓	✓	✓	✓	✓				✓	✓
		Elective-II										
		Elective-III										
		Embedded Systems Lab			✓	✓	✓	✓	✓	✓		✓
		Technical Seminar and Report Writing										
Second	III	SoC design for Embedded System		✓	✓	✓	✓	✓	✓		✓	✓
		Elective-IV										
		Elective-V										
		Project Work Phase-I				✓		✓		✓		✓
	IV	Project Work Phase-II				✓		✓		✓		✓

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ANNA UNIVERSITY, CHENNAI
UNIVERSITY DEPARTMENTS
M.E. VLSI DESIGN AND EMBEDDED SYSTEMS
REGULATIONS – 2015
CHOICE BASED CREDIT SYSTEM
CURRICULA AND SYLLABI
SEMESTER - I

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	MA7152	Advanced Applied Mathematics	FC	4	4	0	0	4
2.	VE7103	Digital Integrated Circuit Design	PC	3	3	0	0	3
3.	VE7104	Introduction to Embedded Controllers	PC	3	3	0	0	3
4.	VE7101	CMOS Analog IC Design	PC	3	3	0	0	3
5.	VE7102	Design for Testability	PC	3	3	0	0	3
6.		Elective-I		3	3	0	0	3
PRACTICALS								
7.	VE7111	Analog and Digital System Design Lab	PC	4	0	0	4	2
			TOTAL	23	19	0	4	21

SEMESTER - II

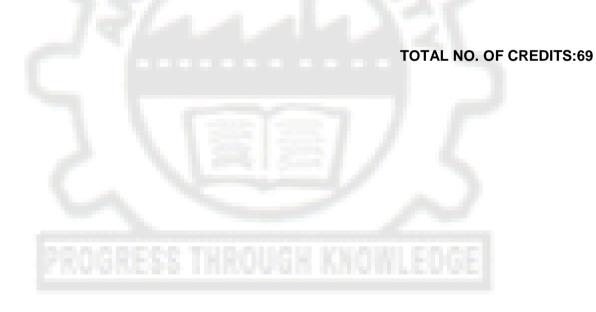| SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	NE7251	Real Time Embedded System	PC	3	3	0	0	3
2.	VE7202	VLSI Architectures for System Design	PC	3	3	0	0	3
3.	VE7201	Hardware Software Co Design of Embedded System	PC	3	3	0	0	3
4.	VL7252	Low Power VLSI Design	PC	3	3	0	0	3
5.		Elective-II	PE	3	3	0	0	3
6.		Elective-III	PE	3	3	0	0	3
PRACTICALS								
7.	VE7211	Embedded Systems Lab	PC	4	0	0	4	2
8.	VE7212	Technical Seminar and Report Writing	EEC	2	0	0	2	1
			TOTAL	24	18	0	6	21

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III SEMESTER

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	VE7301	SoC Design for Embedded System	PC	3	3	0	0	3
2.		Elective-IV	PE	3	3	0	0	3
3.		Elective-V	PE	3	3	0	0	3
PRACTICALS								
4.	VE7311	Project Work Phase – I	EEC	12	0	0	12	6
			TOTAL	**22**	**9**	**0**	**12**	**15**

IV SEMESTER

SL. No	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
PRACTICALS								
1.	VE7411	Project Work Phase – II	EEC	24	0	0	24	12
			TOTAL	**24**	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS:69

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ANNA UNIVERSITY, CHENNAI
UNIVERSITY DEPARTMENTS
M.E. VLSI DESIGN AND EMBEDDED SYSTEMS (PART - TIME)
REGULATIONS – 2015
CHOICE BASED CREDIT SYSTEM
CURRICULA AND SYLLABI I TO VI SEMESTERS

I SEMESTER

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	MA7152	Advanced Applied Mathematics	FC	4	4	0	0	4
2.	VE7103	Digital Integrated Circuit Design	PC	3	3	0	0	3
3.	VE7101	CMOS Analog IC Design	PC	3	3	0	0	3
PRACTICALS								
4.	VE7111	Analog and Digital System Design Lab	PC	4	0	0	4	2
			TOTAL	14	10	0	4	12

II SEMESTER

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	NE7251	Real Time Embedded Systems	PC	3	3	0	0	3
2.	VE7201	Hardware Software Co design of Embedded System	PC	3	3	0	0	3
3.		Elective-I	PE	3	3	0	0	3
PRACTICALS								
4.	VE7211	Embedded Systems Lab	PC	4	0	0	4	2
			TOTAL	13	9	0	4	11

III SEMESTER

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	VE7104	Introduction to Embedded Controllers	PC	3	3	0	0	3
2.	VE7102	Design for Testability	PC	3	3	0	0	3
3.		Elective-II	PE	3	3	0	0	3
4.		Elective-III	PE	3	3	0	0	3
			TOTAL	12	12	0	0	12

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IV SEMESTER

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	VE7202	VLSI Architectures for System Design	PC	3	3	0	0	3
2.	VL7252	Low Power VLSI Design	PC	3	3	0	0	3
3.		Elective-IV	PE	3	3	0	0	3
PRACTICALS								
4.	VE7212	**Technical Seminar and Report Writing**	EEC	2	0	0	2	1
			TOTAL	**11**	**9**	**0**	**2**	**10**

V SEMESTER

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	VE7301	SoC design for Embedded System	PC	3	3	0	0	3
2.		Elective-V	PE	3	3	0	0	3
PRACTICALS								
3.	VE7311	Project Work Phase – I	EEC	12	0	0	12	6
			TOTAL	**18**	**6**	**0**	**12**	**12**

VI SEMESTER

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
PRACTICALS								
1.	VE7411	Project Work Phase II	EEC	12	0	0	24	12
			TOTAL	**12**	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS:69

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FOUNDATION COURSES (FC)

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
PRACTICALS								
1.		Advanced Applied Mathematics	FC	4	4	0	0	4
			TOTAL	**4**	**4**	**0**	**0**	**4**

PROFESSIONAL CORE (PC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.		Introduction to Embedded Controllers	PC	3	3	0	0	3
2.		Digital Integrated Circuit Design	PC	3	3	0	0	3
3.		CMOS Analog IC Design	PC	3	3	0	0	3
4.		Design For Testability	PC	3	3	0	0	3
5.		Real Time Embedded Systems	PC	3	3	0	0	3
6.		VLSI Architectures for System Design	PC	3	3	0	0	3
7.		Hardware - Software Co-design of Embedded system	PC	3	3	0	0	3
8.		Low Power VLSI Design	PC	3	3	0	0	3
9.		SoC design for Embedded System	PC	3	3	0	0	3
10.		Analog & Digital System Design Lab	PC	4	0	0	4	2
11.		Embedded Systems Lab	PC	4	0	0	4	2

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PROFESSIONAL ELECTIVES (PE)

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	NE7072	ASIC Design	PE	3	3	0	0	3
2.	VL7073	VLSI Signal Processing	PE	3	3	0	0	3
3.	VE7016	RF IC Design	PE	3	3	0	0	3
4.	VE7011	MEMS and Microsystems	PE	3	3	0	0	3
5.	VE7013	Nano Electronics	PE	3	3	0	0	3
6.	VE7018	VLSI For Wireless Communication	PE	0	3	0	0	3
7.	VE7015	Parallel and Reconfigurable Architectures	PE	3	3	0	0	3
8.	VE7001	Advanced CMOS Analog IC Design	PE	3	3	0	0	3
9.	NE7074	Computational Intelligence	PE	3	3	0	0	3
10.	AP7073	**Design and Analysis of Computer Algorithms**	PE	3	3	0	0	3
11.	VE7007	Distributed Embedded Computing	PE	3	3	0	0	3
12.	VE7017	Robotics	PE	3	3	0	0	3
13.	VE7002	Advanced Embedded System Design	PE	3	3	0	0	3
14.	NE7071	Adaptive Signal Processing	PE	3	3	0	0	3
15.	VE7014	Network on Chip Design	PE	3	3	0	0	3
16.	VE7009	Embedded C	PE	3	3	0	0	3
17.	VE7003	Algorithm For VLSI Design Automation	PE	3	3	0	0	3
18.	VE7008	Embedded Automotive Systems	PE	3	3	0	0	3
19.	VE7004	Computer Aided Design of VLSI Systems	PE	3	3	0	0	3
20.	VE7005	Design of Embedded Control System	PE	3	3	0	0	3
21.	VE7012	Multi Core Architectures and Programming	PE	3	3	0	0	3
22.	VE7010	Embedded Networking	PE	3	3	0	0	3
23.	NE7076	Digital Image and Video Processing	PE	3	3	0	0	3
24.	VE7006	Digital Signal Processors and Architectures	PE	3	3	0	0	3

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EMPLOYABILITY ENHANCEMENT COURSES (EEC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.		**Technical Seminar and Report Writing**	EEC	2	0	0	2	1
2.		Project Work Phase –I	EEC	12	0	0	12	6
3.		Project Work Phase –II	EEC	24	0	0	24	12

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MA7152   **ADVANCED APPLIED MATHEMATICS**   L T P C
                                                                   4 0 0 4

OBJECTIVES:
- To encourage students to develop a working knowledge of the central ideas of linear algebra;
- To study and understand the concepts of probability and random variable of the various functions;
- To understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete-time Markov chains;
- To formulate and construct a mathematical model for a linear programming problem in real life situation;
- To introduce the Fourier Transform as an extension of Fourier techniques on periodic functions and to solve partial differential equations.

UNIT I   LINEAR ALGEBRA   12
Vector spaces – norms – Inner Products – Eigenvalues using QR transformations – QR factorization - generalized eigenvectors – Canonical forms – singular value decomposition and applications – pseudo inverse – least square approximations --Toeplitz matrices and some applications.

UNIT II   ONE DIMENSIONAL RANDOM VARIABLES   12
Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT III   RANDOM PROCESSES   12
Classification – Auto correlation - Cross correlation - Stationary random process – Markov process –- Markov chain - Poisson process – Gaussian process.

UNIT IV   LINEAR PROGRAMMING   12
Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models.

UNIT V   FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS   12
Fourier transforms: Definitions, properties-Transform of elementary functions, Dirac Delta functions – Convolution theorem – Parseval's identity – Solutions to partial differential equations: Heat equations, Wave equations, Laplace and Poison's equations.

                                                                TOTAL :60 PERIODS
OUTCOMES:
On successful completion of this course, students will be able to
- Classify the random process.
- Formulate and develop a mathematical model for linear programming problem
- Apply the concept of fourier transform to real life situation

REFERENCES:
1. Bronson, R.Matrix Operation, Schaum's outline series, McGraw Hill, Newyork (1989).
2. Oliver C. Ibe, "Fundamentals of Applied Probability and Random Processes, Academic Press, (An imprint of Elsevier), 2010.
3. Taha H.A. "Operations Research : An introduction" Ninth Edition, Pearson Education, Asia,
4. New Delhi 2012.
5. Sankara Rao, K. "Introduction to partial differential equations" Prentice Hall of India, pvt, Ltd,
6. New Delhi, 1997.
7. Andrews,L.C. and Philips.R.L. "Mathematical Techniques for engineering and scientists", Printice Hall of India, 2006.
8. O'Neil P.V. "Advanced Engineering Mathematics", (Thomson Asia pvt ltd, Singapore) 2007,
9. cengage learning India private limited.

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DIGITAL INTEGRATED CIRCUIT DESIGN L T P C
3 0 0 3

OBJECTIVES:
- To study and realize various building blocks of digital VLSI circuits in transistor level.
- To design the architectural choices and performance tradeoffs involved and to realize circuits in CMOS technology.
- To introduce the design knowledge about CMOS testing and its implementation strategies.

UNIT I   MOS TRANSISTOR PRINCIPLES   9
MOS Technology and VLSI, Pass transistors, NMOS, CMOS Fabrication process and Electrical properties of CMOS circuits and Device modeling, Characteristics of CMOS inverter, Scaling principles and fundamental limits. Propagation Delays, CMOS inverter scaling, Stick diagram, Layout diagram, Layout rules, Elmore's constant, Logical Effort.

UNIT II   COMBINATIONAL LOGIC CIRCUITS   9
Static CMOS logic Design, Design techniques to improve the speed, power dissipation of CMOS logic, low power design techniques, Ratioed logic, Pass transistor Logic, Transmission gate logic, CPL, DCVSL, Dynamic CMOS logic, Domino logic, Dual Rail logic, NP CMOS logic and NOR array logic.

UNIT III   SEQUENTIAL LOGIC CIRCUITS   9
Static and Dynamic Latches and Registers, Timing Issues, Pipelines, Clocking strategies, Memory Architectures, and Memory control circuits.

UNIT IV   DESIGNING ARITHMETIC BUILDING BLOCKS & TESTING   9
Datapath circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area tradeoffs.

UNIT V   CMOS TESTING AND IMPLEMENTATION STRATEGIES   9
Need for testing -Manufacturing test – Design for testability – Boundary scan, Full Custom and Semicustom Design, FPGA building block architectures, FPGA interconnects.

                                                           TOTAL:45 PERIODS
OUTCOMES:
After completion of this course:
- Ability to expand their knowledge in designing circuit level implementation to realize and test system based architectures, which include digital, memory, and mixed-signal subsystems.

REFERENCES:
1. Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated circuits: A design perspective". Second Edition, Prentice Hall of India, 2003.
2. N.Weste, K.Eshraghian, "Principles of CMOS VLSI DESIGN", A system Perspective, second edition,Addision Wesley 1993.
3. A.Pucknell, Kamran Eshraghian, "BASIC VLSI DESIGN", Third edition, Prentice
4. Hall of India, 2007.
5. M.J. Smith, "Application specific integrated circuits", Addisson Wesley, 1997.
6. R.Jacob Baker, Harry W.LI., David E.Boyee, "CMOS Circuit Design, Layout and Simulation", 2005 Prentice Hall of India.

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VE7104   INTRODUCTION TO EMBEDDED CONTROLLERS   L T P C
                                                                   3 0 0 3

OBJECTIVES:
- To learn about the designing of an embedded system for commercial applications.
- To learn the features, architecture and programming of PIC and ARM microcontrollers
- To study the interfacing peripherals with microcontrollers.
- To learn about the communication protocols in a Microcomputer system.
- To learn about the fundamentals of real-time operating system in an embedded system.

UNIT I   INTRODUCTION TO EMBEDDED SYSTEMS   9
Processor Embedded into a System, Embedded Hardware Units and Devices in a System, Embedded Software in a System, Examples of Embedded Systems, Embeded System on-chip (Soc) and Use of VLSI Circuit Design Technology, Complex Systems Design and Processors, Design Process in Embedded Systems, Formalization of System Design, Design Process and Design Examples, Classification of Embedded Systems.

UNIT II   PIC MICROCONTROLLERS   9
PIC 16F877 MCU, Architecture, Features, Memory and memory map, I/O ports, Timers and CCP Devices, ADC, Interrupts, Instruction format, Addressing Modes, Instruction Set, Programming with MPLAB IDE.

UNIT III   ARM BASED MICROCONTROLLERS   9
Introduction to 16 bit Processors, ARM Architecture, ARM cortex M3, 16 bit ARM Instruction set, Thumb Instruction set, Exception Handling in ARM, Porting Linux in ARM, Assembly and C programming.

UNIT IV   INTERFACING I/O DEVICES AND COMMUNICATION PROTOCOLS   9
LED, liquid crystal display, Motor (DC, Servo, Stepper), Relays, Keypad, Keyboard, Touch screen, Sensors (thermocouple, force, displacement), SD card, Infrared connectivity, Serial communication protocols (UART, I2C, SPI, CAN, USB, LIN), Parallel communication protocols (PCI, ISA), Wireless communication networks (Bluetooth, Xbee, Wifi, GSM), Global positioning system receivers, Embedded Systems and the internet.

UNIT V   MULTITASKING AND THE REAL-TIME OPERATING SYSTEM   9
The challenges of multitasking and real-time, Achieving multitasking with sequential programming, RTOS, Scheduling and the scheduler, Developing tasks, Data and resource protection- the semaphore,Examples using Salvo Real-time operating systems.

                                                              TOTAL:45 PERIODS
OUTCOMES:
After completion of this course:
- Students will be able to interface peripherals with microcontrollers.
- Students will be able to design an embedded system in real time.
- Students will be able to use the communication protocols in application specific.

REFERENCES:
1. Raj Kamal, "Embedded Systems- Architecture, Programming and Design", Second Edition, Tata McGraw-Hill Publications, 2008.
2. Yifeng Zhu,"Embedded Systems with ARM Cortex-M3 Microcontrollers in Assembly Language and C**",** E-Man Press LLC; 1st edition, 2014.
3. Tim Wilmshurst, "Designing Embedded Systems with PIC microcontrollers-Principles and Applications", Newnes Publications, 2007.
4. Julio Sanchez Maria P.Canton, "Microcontroller Programming: The microchip PIC", CRC Press, Taylor & Francis Group,2007.
5. Martin Bates, "Interfacing PIC microcontrollers-Embedded Design by Interactive Simulation", Newnes Publication, 2006.
6. Muhammad Ali Mazidi, Rolin McKinlay, Danny Causey, "PIC Microcontroller and Embedded Systems: Using Assembly and C for PIC18", Prentice Hall publications, 2007.

VE7101   **CMOS ANALOG IC DESIGN**   **L T P C**
                                                                          3 0 0 3

OBJECTIVES:
- The course will discuss the equivalent circuits and models of MOS circuits.
- To analyze bias circuits using CMOS current mirrors.
- To design and analyze the frequency response of multistage differential amplifiers.
- To discuss the stability and frequency compensation of feedback amplifiers.

UNIT I   SINGLE STAGE AMPLIFIERS   9
Review of MOS physics and equivalent circuits and models. Large and Small signal analysis CS, CG and source follower, miller effect, frequency response of CS, CG and source follower.

UNIT II   CURRENT MIRRORS   6
Current Sources, Basic Current Mirrors, Cascode stages for Current mirrors , Wilson Current Mirror, Large and small signal analysis of current mirrors.

UNIT III   MULTISTAGE DIFFERENTIAL AMPLIFIERS   12
Differential amplifier, Large and small signal analysis of the balanced differential amplifier, device mismatches in differential amplifier, small and large signal analysis of the differential pair with current mirror load, $PSRR^+$, $PSRR^-$ and CMRR of differential amplifiers, small signal analysis of telescopic amplifier, two-stage amplifier and folded cascaded amplifier.

UNIT IV   FREQUENCY RESPONSE OF MULTISTAGE DIFFERENTIAL
**   AMPLIFIERS   9**
Dominant-Pole approximation, zero-value time constant analysis, - Frequency response of current mirror loaded, differential amplifier, short circuit time constants, frequency response of telescopic cascaded, folded cascode amplifier.

UNIT V   STABILITY AND FREQUENCY COMPENSATION OF FEEDBACK
**   AMPLIFIERS   9**
Properties and types of negative feedback circuits, feedback configurations, effect of loading in feedback networks, feedback circuit analysis using return ratio- modelling input and output port in feedback network, the relation between gain and bandwidth in feedback amplifiers, phase margin, frequency compensation, compensation of two stage MOS amplifiers.

**   TOTAL:45 PERIODS**
OUTCOMES:
After completion of this course, students are expected to:
- Be able to analyze and design CMOS analog IC building blocks like MOS amplifiers, current mirrors and multistage differential amplifiers.

REFERENCES:
1. Gray, Hurst, Lewis, Meyar, "Analysis and Design of Analog Integrated Circuits" Fifth Edition John Wiley, 2009.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Twelfth Reprint, Tata McGraw Hill, 2012.
3. Phillip E. Allen, Douglas R.Holberg, "CMOS Analog Circuit Design", Third edition, Oxford University Press, 2011.
4. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010.

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VE7102   **DESIGN FOR TESTABILITY**   **L T P C**
                                                                             3 0 0 3

OBJECTIVES:
- To describe the various fault models and to understand the fundamentals of fault detection.
- To understand the difficulties of sequential circuit tests.
- To understand the basic principles of test vector generation and to describe the basic principles of testable circuit design.
- To understand the principles of built in self test and boundary scan standard
- To discuss the structured design for testability techniques for system-on-a-chip design and automatic test equipment.

UNIT I   INTRODUCTION TO TESTING   9
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing. VLSI testing process, types of testing, Automatic test Equipment, Delay Test.

UNIT II   FAULT MODELLING AND SIMULATION   9
Defects, errors, Faults, Functional versus Structural testing, Levels of Fault models, Single stuck-at-fault - Modelling circuits for Simulation, Algorithms for True Value and Fault simulation, Statistical methods for Fault simulation.

UNIT III   ATPG FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS   9
Combinational Circuit: Algorithms and Representations, Redundancy Identification (RID), Significant Combinational ATPG Algorithms - D-Calculus and D-Algorithm, PODEM, FAN, Advanced Algorithms - Test Generation Systems, Test Compaction.
Sequential Circuit: ATPG for Single-Clock Synchronous Circuits, Time-Frame Expansion Method, Simulation-Based Sequential Circuit ATPG -CONTEST Algorithm, Genetic Algorithms.

UNIT IV   BUILT-IN SELF-TEST & BOUNDARY SCAN STANDARD   9
Ad-Hoc DFT Methods and Scan Design, Economic Case for BIST, Random Logic BIST, Memory BIST, Delay Fault BIST - Purpose of Standard, System Configuration with Boundary Scan, Boundary Scan Description Language.

UNIT V   SYSTEM TEST AND CORE-BASED DESIGN   9
System Test Problem Defined, Functional Test, Diagnostic Test, Testable System Design, Core-Based Design and Test-Wrapper, Test Architecture for System-on-a-Chip (SOC), Integrated Design and Test Approach.

                                                                    TOTAL:45 PERIODS
OUTCOMES:
After completion of this course, students are:
- Well equipped with the concepts of testable circuit designs and testability techniques for system-on-a-chip design and automatic test equipment.

REFERENCES:
1. M.L. Bushnell, V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory, and Mixed Signal VLSI Circuits - Kluwer Academic Publishers, 2002.
2. Samiha Mourad, Yervant Zorian, "Principles of Testing Electronic Systems", A Wiley Interscience Publications, 2002.
3. Alexander Miczo, "Digital Logic Testing and Simulation", Second Edition, A John Wiley & Sons Inc. Publication, 2003.
4. Abramovici, M, Breuer, M.A and Friendman, A.D., Digital systems and Testing and Testable Design, Computer Science Press 1990.
5. Alfred Crouch, Design for test for digital IC & Embedded Core Systems, Prentice Hall, 2002
6. L.T. Wang, C.W. Wu and X. Wen, VLSI Test Principles and Architectures, Elsevier, 2006.
7. Alfred L. Crouch, Design-for-Test for Digital IC's and Embedded Core Systems, Prentice Hall PTR.

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VE7111 **ANALOG AND DIGITAL SYSTEM DESIGN LAB** **L T P C**
                                                       0 0 4 2

OBJECTIVES:
- To understand the various analog and digital circuits and their simulation using Cadence tool.
- To learn the advanced concepts of modern VLSI circuit and system design
- To design common sequential functions: flip-flops, registers, latches, and state-machines.
- To understand placement, routing, and verify timing of a standard cell design.

DIGITAL DESIGN LAB WITH CADENCE:
1. HDL based design entry and simulation of Parameterizable cores of Counters, Shift registers, State machines, 8-bit Parallel adders and 8 –Bit multipliers.
2. HDL based design entry and simulation of Parameterizable cores on the simple Distributed Arithmetic system.
3. HDL based design entry and simulation of Parameterizable cores on memory design and 4 – bit ALU.
4. Synthesis, P&R and post P&R simulation, Critical paths and static timing analysis results to be identified.

ANALOG IC DESIGN WITH CADENCE VIRTUOSO:
Circuit simulation, Layout generation, parasitic extraction, Synthesis and Standard cell based design of the circuits. Identification of critical paths, power consumption. P&R, power and clock routing, post P&R simulation and Static timing analysis of:
1. Design of CMOS Inverter - Circuit Simulation, transfer characteristic curve, transient analysis, Layout design.
2. Design of Current Mirrors - Simple current source generator, Current mirror, Wilson Current mirror circuit, Layout of the current mirror circuit.
3. A simple differential amplifier. Measure gain, ICMR, and CMRR - Differential input, single ended differential amplifier design, Differential amplifier design, telescopic amplifier design, layout of differential amplifier.

TOTAL : 60 PERIODS

OUTCOMES:
After the completion of this lab, Students should be able:
- To create the hierarchical decomposition of sequential designs.
- To perform synthesis and analysis of combinational and sequential designs.

NE7251 **REAL TIME EMBEDDED SYSTEM** **L T P C**
                                            3 0 0 3

OBJECTIVES:
- To understand the basics of embedded system, architecture of PIC microcontroller and ARM processor.
- To understand the RTOS concepts like scheduling and memory management related to the embedded system.
- To learn the protocols of embedded wireless application.
- To understand concepts involved in the design of hardware and software components for an embedded system.

UNIT I   **INTRODUCTION**   **12**
Real Time System – Embedded Systems – Architecture of Embedded System - Simple Programming for Embedded System – Process of Embedded System Development - Pervasive Computing – Information Access Devices – Smart Cards – Microcontrollers – ARM Processor - Real time Microcontrollers – Low power embedded systems, microcontrollers & RF.

UNIT II   EMBEDDED/REAL TIME OPERATING SYSTEM   9
Operating System Concepts: Processes, Threads, Interrupts, Events - Real Time Scheduling Algorithms - Memory Management – Overview of Operating Systems for Embedded, Real Time, Handheld Devices – Target Image Creation – Programming in Linux, RTLinux, VxWorks, uC/Os overview.

UNIT III   CONNECTIVITY   9
Wireless Connectivity - Bluetooth – Other short Range Protocols – Wireless Application Environment – Service Discovery – Middleware.

UNIT IV   REAL TIME UML   6
Requirements Analysis – Object Identification Strategies – Object Behaviour – Real Time Design Patterns.

UNIT V   SOFTWARE DEVELOPMENT AND CASE STUDY   9
Concurrency – Exceptions – Tools – Debugging Techniques – Optimization – Case Studies - Interfacing Digital Camera with USB port and Data Compressor.

TOTAL: 45 PERIODS

OUTCOMES:
- To be able to make a choice a suitable embedded processor for a given application.
- To be able to design the hardware and software for the embedded system.
- To be able to design and develop the real time kernel/operating system functions, task control block structure and analyze different task states.
- To be able to implement different types of inter task communication and synchronization techniques.

REFERENCES:
1. R.J.A.Buhr, D.L.Bailey, "An Introduction to Real-Time Systems", Prentice-Hall International, 1999.
2. David E-Simon, "An Embedded Software Primer", Pearson Education, 2007.
3. C.M.Krishna, Kang G.Shin, "Real Time Systems", Mc-Graw Hill, 1997.
4. B.P.Douglass, "Real Time UML", 2nd Edition, Addison-Wesley 2000.
5. Dr.K.V.K.K.Prasad, "Embedded/Real Time Systems: Concepts, Design and Programming", DreamTech Press, Black Book, 2005.
6. R.Barnett, L.O.Cull, S.Cox, "Embedded C Programming and the Microchip PIC", Thomason Learning, 2004.
7. Wayne Wolf, "Computers as Components - Principles of Embedded Computer System Design", Mergen Kaufmann Publisher, 2006.
8. Sriram V Iyer, Pankaj Gupta, "Embedded Real Time Systems Programming", Tata Mc-Graw Hill, 2004.

VE7202   **VLSI ARCHITECTURES FOR SYSTEM DESIGN**   L T P C
                                                          3 0 0 3

OBJECTIVES:
- This course will introduce the features, programming and applications of programmable logic devices.
- Provide VLSI system design experience using FSM.
- Discuss the various implementation strategies with FPGA.

UNIT I   PROGRAMMABLE LOGIC   9
ROM, PLA, PAL, PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series, CPLD, Cypres FLASH 370 Device Technology, Lattice LSI's Architectures – 3000 Series – Speed Performance and in system programmability.

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UNIT II   FPGAS: FIELD PROGRAMMABLE GATE ARRAYS   9

Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs, Case studies – Xilinx Virtex-6, Spartan-6 FPGAs, ALTERA's FLEX 8000/10000 FPGAs, NIOS II Embedded Processor, ACTEL's IGLOO series, ProASIC3 series FPGAs.

UNIT III   FINITE STATE MACHINES (FSM)   9

Top Down Design – State Transition Table, state assignments for FPGAs. Problem of initial state assignment for one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL. Alternative realization for state machine chart using microprogramming. Linked state machines. One – Hot state machine, Petrinetes for state machines – basic concepts, properties. Extended petrinets for parallel controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT IV   FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN   9

Architectures centered around non-registered PLDs. State machine design centered around shift registers. One – Hot design method. Use of ASMs in One – Hot design. K Application of One – Hot method. System level design – controller, data path and functional partition.

UNIT V   IMPLEMENTING APPLICATIONS WITH FPGAS   9

Strengths and Weaknesses of FPGAs, Application and computational Characteristics and Performance - General Implementation Strategies for FPGA-based Systems - Configure-once Runtime Reconfiguration Design Flow –.Implementing Arithmetic - Fixed-point, Floating- point, Block Floating Point number Representation - CORDIC Architectures for FPGA Computing.

TOTAL:45 PERIODS

OUTCOMES:

After the completion of this course, the students are to:
- Be able to make the system level designs using FSM and analyze the performance with FPGA.

REFERENCES:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte), 1994.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic
3. Publications, 1994.
4. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
5. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
6. Scott Hauck and Andre DeHon Reconfigurable Computing The Theory and Practice of FPGA based Computation Morgan Kaufmann Publishers

VE7201	HARDWARE SOFTWARE CO DESIGN OF EMBEDDED SYSTEM	L	T	P	C
		3	0	0	3

OBJECTIVES:
- To introduce the key concepts of hardware/software communication to make trade-offs between the flexibility and the performance of a digital system.
- To learn the concept of integration of custom hardware components with software.
- Students will gain design and implementation experience with case studies.
-

UNIT I   NATURE OF HARDWARE AND SOFTWARE   9

Hardware, Software, Definition of Hardware/Software Co-Design – Driving factors Platform design space – Application mapping – Dualism of Hardware design and software design – Concurrency and parallelism, Data flow modeling and Transformation – Data Flow Graph – Tokens, actors and queues, Firing rates, firing rules and Schedules – Synchronous data flow graph – control flow modeling – Adding time and resources – Trandformations.

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UNIT II   DATA FLOW IMPLEMENTATION IN SOFTWARE AND HARDWARE   9

Software Implementation of Data Flow – Converting queues and actors into software, Dynamic Scheduler – Hardware Implementation of Data Flow – single rate SDF graphs into hardware, Pipelining – Analysis of control flow and data flow – construction of control and data flow graph – Translating C into hardware – Designing data path and controller.

UNIT III   DESIGN SPACE OF CUSTOM ARCHITECTURES   9

Finite state machines with datapath – FSMD design example, Limitations – Microprogrammed Architecture – Microprogrammed control, microinstruction encoding, Microprogrammed data path, microprogrammed machine – General purpose Embedded Core – RISC pipeline, Program organization – SoC interfaces for custom hardware – Design Principles in SoC Architecture

UNIT IV   HARDWARE/ SOFTWARE INTERFACES   9

Principles of Hardware/software communication – synchronization schemes, communication constrained versus Computation constrained, Tight and Loose coupling - On-chip buses – Memory mapped interfaces – coprocessor interfaces – custom instruction interfaces – Coprocessor hardware interface – Data and control design, programmer's model.

UNIT V   CASE STUDIES   9

Trivium Cripto coprocessor – Trivium stream cipher algorithm, Trivium for 8-bit platforms – AES coprocessor, CORDIC coprocessor – algorithm and implementation.

TOTAL:45 PERIODS

OUTCOMES:
On completion of the course, a student should be able:
* To analyze and apply design methodologies.
* To appreciate the fundamental building blocks of the using hardware and software co-design and related implementation and testing environments and techniques and their interrelationships.
* To be familiar with modern hardware/software tools for building prototypes and to be able to demonstrate practical competence in these areas

REFERENCES:
1. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub, 1997.
3. Giovanni De Micheli, Rolf Ernst Morgon, "Reading in Hardware/Software Co-Design" Kaufmann Publishers, 2001.
4. Patrick Schaumont, A Practical Introduction to Hardware/Software Codesign, 2nd Edition, Springer, 2010.

VL7252	LOW POWER VLSI DESIGN	L T P C
		3 0 0 3

OBJECTIVES:
* Identify sources of power in an IC.
* Identify the power reduction techniques based on technology independent and technology dependent power dissipation mechanism in various MOS logic style.
* Identify suitable techniques to reduce the power dissipation and design memory circuits with low power dissipation.

UNIT I   POWER DISSIPATION IN CMOS   9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

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UNIT II POWER OPTIMIZATION 9
Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9
Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION 9
Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9
Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

OUTCOMES:
- The student will get to know the basics and advanced techniques in low power design which is a hot topic in today's market where the power plays major role.
- The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

REFERENCES:
1. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer, 2002.
3. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995.
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons, inc. 2001.

VE7211	EMBEDDED SYSTEMS LAB	L T P C
		0 0 4 2

OBJECTIVES:
- Students have knowledge about the basic functions of embedded systems.
- Students have knowledge in programming skills.

EXPERIMENTS :
ARM/ PIC Microcontroller based Experiments with MPLAB IDE from Microchip/ µVision IDE for ARM programming from Keil:

1. Interfacing basic digital input output devices.
2. Interfacing a character LCD.
3. Interfacing A/D and D/A converter.
4. Interfacing Capture/Compare/PWM module.
5. DC motor control.
6. Multiplexing seven segment LED displays.
7. Interfacing Stepper motor and temperature sensor.
8. Traffic light controller using Keil real time Kernel.

TOTAL : 60 PERIODS

OUTCOMES:
- An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, and sustainability.

VE7301	SoC DESIGN FOR EMBEDDED SYSTEM	L T P C
		3 0 0 3

OBJECTIVES:
- To introduce architecture and design concepts underlying system on chips.
- Students can gain knowledge of designing SoCs.
- To impart knowledge about the hardware-software design of a modest complexity chip all the way from specifications, modeling, synthesis and physical design.

UNIT I   SYSTEM ARCHITECTURE: OVERVIEW   9
Components of the system – Processor architectures – Memory and addressing – system level interconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.

UNIT II   PROCESSOR SELECTION FOR SOC   9
Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interrupts and exceptions. Basic elements in instruction handling – Minimizing pipeline delays – reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.

UNIT III   MEMORY DESIGN   9
SoC external memory, SoC internal memory, Scratch pads and cache memory – cache organization and write policies – strategies for line replacement at miss time – split I- and D-caches – multilevel caches – SoC memory systems – board based memory systems – simple processor/memory interaction.

UNIT IV   INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION   9
Bus architectures – SoC standard buses – AMBA, CoreConnect – Processor customization approaches – Reconfigurable technologies – mapping designs onto reconfigurable devices - FPGA based design – Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing.

UNIT V   FPGA BASED EMBEDDED PROCESSOR   9
Hardware software task partitioning – FPGA fabric Immersed Processors – Soft Processors and Hard Processors – Tool flow for Hardware/Software Co-design –Interfacing Processor with memory and peripherals – Types of On-chip interfaces – Wishbone interface, Avalon Switch Matrix, OPB Bus Interface, Creating a Customized Microcontroller - FPGA-based Signal Interfacing and Conditioning.

TOTAL:45 PERIODS

OUTCOMES:
Upon successful completion of the program the students shall
- Explain all important components of a System-on-Chip and an embedded system, i.e. digital hardware and embedded software;
- Outline the major design flows for digital hardware and embedded software;
- Discuss the major architectures and trade-offs concerning performance, cost and power consumption of single chip and embedded systems;

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REFERENCES:
1. Michael J. Flynn and Wayne Luk**,** "Computer System Design: System-on-Chip", John Wiley and sons, 2011.
2. Rahul Dubey, "Introduction to Embedded System Design Using Field Programmable Gate Arrays", Springer Verlag London Ltd., 2009.
3. Sudeep Pasricha and Nikil Dutt, On-Chip Communication Architectures - System on Chip Interconnect, Elsevier, 2008.

NE7072	ASIC DESIGN	L T P C
		3 0 0 3

OBJECTIVES:
- To study the basic concepts of digital CMOS Application Specific Integrated Circuit (ASIC) systems design and library cell design.
- To know the architectural details of programmable ASICs.
- To present the ASIC physical design flow, including logic synthesis, floor-planning, placement and routing.
- To know back-end physical design flow steps through VLSI CAD tools.

UNIT I   INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN   9
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

**UNIT II   PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND
              PROGRAMMABLE ASIC I/O CELLS   9**
Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

**UNIT III   PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN
               SOFTWARE AND LOW LEVEL DESIGN ENTRY   9**
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 – Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level
design language - PLA tools -EDIF- CFI design representation.

UNIT IV   LOGIC SYNTHESIS, SIMULATION AND TESTING   9
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V   ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING   9
System partitioning - partitioning methods - floor planning - placement - physical design flow – Routing - global routing - detailed routing - special routing - circuit extraction -DRC.

TOTAL:45 PERIODS

OUTCOMES:
Upon completion of this course, the students will:
- Be able to design the ASIC implementation using programmable ASIC devices.
- Be able to comprehend the different issues related to the development of ASIC designs including logic synthesis, floor-planning, placement and routing, tools and future trends.

REFERENCES:
1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997, Reprint 2004.
2. Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical   Approach, Prentice Hall PTR, 2003.

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3. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004
4. R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House Publishers, 2000
5. F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs), Prentice Hall PTR, 1999.

VL7073	VLSI SIGNAL PROCESSING	L T P C
		3 0 0 3

OBJECTIVES:
- This course will introduce approaches and methodologies for VLSI design of signal processing.
- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm,Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL: 45 PERIODS

OUTCOME:
- Students will be able to modify the existing or new DSP architectures suitable for VLSI

REFERENCES:
1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
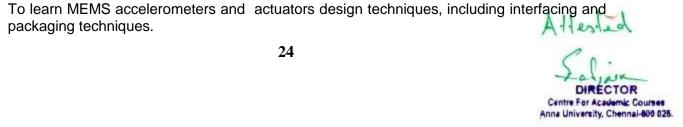2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

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VE7016   **RF IC DESIGN**   **L T P C**
                                                                    3 0 0 3

OBJECTIVES:
- To understand the fundamentals of RF integrated circuits operating at microwave frequencies.
- To learn RFIC design techniques, including system architecture, key building blocks design methodologies in CMOS technology.

UNIT I   COMPONENTS FOR RF IC   9
MOSFET Physics: Long channel and Short channel approximation, Noise: Two port Noise theory,MOS capacitor, Spiral Inductors, Model for on chip inductors,Bond wire inductors, Monolithic transformer realization, Interconnects.

UNIT II   CIRCUIT DESIGN FOR LOW NOISE AMPLIFIERS   9
Methods of Open circuit and Short circuit time constants, Bandwidth enhancers, Tuned amplifier, Nuetralisation, cascaded amplifiers, CMOS amplifiers, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III   POWER AMPLIFIER DESIGN   9
Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, Class A, AB, B, C, D, E and F amplifiers, Linearization Techniques, RF power amplifier design example.

UNIT IV   PLL AND FREQUENCY SYNTHESIZERS   9
Linearized PLL Model, Noise properties, Phase detectors, Loop filters and Charge pumps, PLL Design examples. Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

UNIT V   SYSTEM ARCHITECUTRE   9
Receiver architecture: Noise figure, Linearity in cascaded systems,Single and Dual conversion receivers, Image reject receivers, Direct conversion. Transmitter architectures, Detailed Chip design example: WLAN Transceiver architecture.

                                                      TOTAL: 45 PERIODS
OUTCOMES:
- Ability to analyze the high frequency effects on basic circuit components.
- Ability to design RF LNAs and receivers.
- Ability to design RF power amplifiers.
- Ability to design PLL and frequency synthesizers

REFERENCES:
1. Thomas Lee, "The Design of Radio Frequency CMOS Integrated Circuits", Cambridge University Press, 2nd Edition, Cambridge, 2004.
2. Matthew M.Radmanesh "RF and Microwave Design Essentials", AuthorHouse, Bloomington, 2007.
3. John W.M.Rogers and Calvin Plett, "Radio Frequency Integrated Circuit Design", 2nd Edition, Artech House, Norwood, 2010.
4. Devendra.K. Misra, "Radio Frequency and Microwave Communication Circuits – Analysis and Design", John Wiley and Sons, Newyork, 2004.

VE7011   **MEMS AND MICROSYSTEMS**   **L T P C**
                                                                    3 0 0 3

OBJECTIVES:
- To understand the fundamentals of MEMS and Microsystems.
- To learn MEMS accelerometers and actuators design techniques, including interfacing and packaging techniques.

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UNIT I INTRODUCTION TO MEMS 9
MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II MICROMECHANICS 9
Elasticity, Stress, strain and material properties, Bending of thin films, Spring configurations, torsion deflection, Mechanical vibration, Resonance, Thermomechanics - actuators, force and response time, Fracture and thin film mechanics.

UNIT III MICROACTUATORS 9
Electrostatics: basic theory, electrostatic instability. Surface tension, Gap and finger pull up, Electrostatic actuators, comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators, bistable actuators.

UNIT IV INTERFACING AND PACKAGING 9
Electronic Interfaces, Feedback systems, Noise, Packaging: Dicing-Wafer level Packaging-Wafer bonding-Connections between layers-self assembly-higher level of packaging.

UNIT V CASE STUDIES 9
Optical MEMS, RF MEMS- System design basics, Case studies: Capacitive accelerometer, Peizo electric pressure sensor, MEMS scanners, Capacitive RF MEMS switch, performance issues.
TOTAL: 45 PERIODS

OUTCOMES:
Upon completion of the course, students will have:
- An ability to analyze the working of MEMS and Microsystems components.
- An ability to design the MEMS accelerometer and to design Electrostatic actuators.
- An ability to analyze the working of RF and Optical MEMS.

REFERENCES:
1. Stephen D Senturia, "Microsystems Design", 2nd edition Springer Publishers, 2005.
2. Nadim Maluf and Kirt Williams, "Introduction to Microelectromechanical Systems Engineering", Artech House, 2004.
3. Mohamed Gad-el-Hak, Editor, "The MEMS Handbook", 2nd Edition, CRC press, 2005.
4. Tai - Ran Hsu, "MEMS and Micro Systems: Design, Manufacture and Nanoscale Engineering", 2nd Edition, Tata McGraw Hill, New Delhi, 2008.

VE7013	NANO ELECTRONICS	L T P C
		3 0 0 3

OBJECTIVES:
- To discuss the fundamentals of nanoelectronics and nanocomputer architectures.
- To impart knowledge about the concepts of nano fabrication, nanostructures and nano phase materials.
- To describe the principle and the operation of nanoelectronic devices.
- To explain the principle and application of spintronic devices.

UNIT I INTRODUCTION 9
Recent past, the present and its challenges, Future, Overview of basic Nano electronics.

UNIT II NANO ELECTRONICS & NANOCOMPUTER ARCHITECTURES 9
Introduction to Nanocomputers, Nanocomputer Architecture, Quantum DOT cellular Automata (QCA), QCA circuits, Single electron circuits, molecular circuits, Logic switches – Interface engineering – Properties (Self-organization, Size-dependent) – Limitations.

UNIT III   NANOELECTRONIC ARCHITECTURES   9

Nanofabrication – Nanopatterning of Metallic/Semiconducting nanostructures (e-beam/X-ray, Optical lithography, STM/AFM- SEM & Soft-lithography) – Nano phase materials – Selfassembled Inorganic/Organic layers.

UNIT IV   SPINTRONICS   9

Introduction, Overview, History & Background, Generation of Spin Polarization Theories of spin Injection, spin relaxation and spin dephasing, Spintronic devices and applications, spin filters, spin diodes, spin transistors. Memory Devices And Sensors.

UNIT V   MEMORY DEVICES AND SENSORS   9

Nano ferroelectrics – Ferroelectric random access memory –Fe-RAM circuit design –ferroelectric thin film properties and integration – calorimetric -sensors – electrochemical cells – surface and bulk acoustic devices – gas sensitive FETs – resistive semiconductor gas sensors –electronic noses – identification of hazardous solvents and gases – semiconductor sensor array.

TOTAL: 45 PERIODS

OUTCOMES:

* Ability to Ddscuss the fundamentals of nanoelectronic architectures and its components.
* Ability to expplain the principles of nanoelectronics, nanodevices, spintronics and molecular electronics.

REFERENCES:

1) Karl Goser, **"**Nanoelectronics & Nanosystems", From Transistors to Molecular and Quantum Devices, 2003.
2) Rainer Waser, "Nanoelectronics and Information Technology" 3rd Edition, Wiley Publications, 2012.

VE7018   **VLSI FOR WIRELESS COMMUNICATION**   **L T P C**
                                                                      3 0 0 3

OBJECTIVES:

* To cover the design of VLSI circuits used in modern wireless transceivers.
* To illustrate the design trade-offs in the transceivers with practical, real life circuit examples, with low power as an important design objective.
* To discuss the architectures of wireless transceivers at the transistor level, using submicron CMOS.
* To discuss the circuits such as low noise amplifiers, mixers, power amplifiers, oscillators, phase locked loops and A/D and D/A converters.

UNIT I   COMMUNICATION CONCEPTS   9

Wireless systems, Standards, Access methods, Modulation schemes, Classical channel, Wireless Channel Description, Path Loss, Multipath Fading, Channel Model and Envelope Fading, Frequency Selective and Fast Fading.

UNIT II   TRANSMITTER AND RECEIVER ARCHITECTURES: 9

Transmitter backend, Quadrature LO generator, Receiver Front End:, Filter Design, Rest of Receiver Front End, Derivation of NF, IIP3 of Receiver Front End - Wideband LNA Design, Narrow Band LNA:, Impedance Matching, Core Amplifier.

UNIT III   ACTIVE AND PASSIVE MIXER   9

Active Mixer: Balancing, Qualitative Description of the Gilbert Mixer, Distortion, Low Frequency Case: Analysis of Gilbert Mixer, Distortion, High Frequency Case, Noise

Passive Mixer: Switching Mixer, Distortion in Unbalanced Switching Mixer, Conversion Gain in Unbalanced Switching Mixer, Noise in Unbalanced Switching Mixer, practical Unbalanced Switching Mixer, Sampling Mixer, Conversion Gain in Single-Ended Sampling Mixer.

UNIT IV   ANALOG-TO-DIGITAL CONVERTERS   9
Demodulators, A/D converters Used in a Receiver, Low-Pass Sigma-Delta Modulators, Implementation of Low-Pass Sigma-Delta Modulators, Bandpass Sigma-Delta Modulators, Implementation of Bandpass Sigma-Delta Modulators.

UNIT V   FREQUENCY SYNTHESIZER: 9
PLL based frequency synthesizer, Phase detector/Charge pump, VCO, Dividers, Ring oscillators, Loop filter – General description, Design approaches.

TOTAL: 45 PERIODS

OUTCOMES:
- Ability to design wireless transceivers using low noise amplifiers, mixers, power amplifiers, oscillators, phase locked loops, A/D and D/A converters and frequency synthesizers.

REFERENCES:
1. Bosco Leung, "VLSI for Wireless Communication, Second Edition, Springer,2011.
2. Emad N Farag, M.I Elmasry, "Mixed Signal VLSI Wireless Design Circuits and Systems", Kluwer Publications, 2000.
3. David Tsee, Pramod Viswanath," Fundamentals of Wireless Communication", Cambridge Univ Press.

VE7015   PARALLEL AND RECONFIGURABLE ARCHITECTURES   L T P C
3 0 0 3

OBJECTIVES:
- The student shall develop an overview and deeper insight into the research and development that is underway to meet future needs of flexible processor solution, for energy efficient reconfigurable architectures with high computing performance.

UNIT I   INTRODUCTION   9
Reconfigurable Computing Systems (RCS) – Evolution of reconfigurable systems – Characteristics of RCS - Advantages and issues, Fundamental concepts & Design steps, Domain specific processors, Application specific processors, Classification of reconfigurable architecture - fine, coarse grain & hybrid architectures

UNIT II   PARALLEL AND ADVANCED PROCESSORS   9
Classification of parallel computers, Multiprocessors and multicomputer, SIMD Processing Architectures, CISC & RISC Processors, VLIW Architectures

UNIT III   RECONFIGURABLE ARCHITECTURES   9
FPGA Technology and Architectures – LUT devices and mapping (Look-up Table) ALU design – Placement and partitioning algorithms – Routing algorithms, Spatial Computing Architectures – Systolic Architectures and Algorithms Systolic Structures

UNIT IV   RECONFIGURATION MANAGEMENT   9
Reconfiguration, Configuration Architectures, Managing the Reconfiguration Process, Reducing Configuration Transfer Time

Attested

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UNIT V   CASE STUDIES OF FPGA APPLICATIONS   9

Dynamic Partial Reconfigurable FIR Filter Design, Trigonometric Computing, Embedded in a Dynamically Reconfigurable CORDIC System-on-Chip, A Fast Run Time Reconfigurable Platform for Image Edge Detection, Efficient Floating-Point Implementation of High-Order (N) LMS Adaptive Filters in FPGA, Area/Performance Improvement of NoC Architectures.

TOTAL: 45 PERIODS

OUTCOMES:

Upon successful completion of the course, the student should be able to:

- Analyze the different architecture principles relevant in parallel and reconfigurable systems.
- Compare the tradeoffs that are necessary to meet the area, power and timing criteria of these systems.
- In depth analysis of current research projects to get broader context and assess its significance.
- Describe and relate new architectures and applications in relations to the previously existing solutions.

REFERENCES:

1. Christophe Bobda, "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications", Springer 2007
2. Scott Hauck and Andre Dehon, "Reconfigurable Computing: The Theory and Practice of FPGA based Computation", Elseiver 2008
3. Niccolo Battezzatti, Luca Sterpone, Massimo Violante, "Reconfigurable Field Programmable Gate Arrays for Mission-Critical Applications", Springer 2011.
4. Kai Hwang, "Advanced computer architecture – Parallelism, Scalability, Programmability"; Tata McGraw Hill Publishing company Ltd., New Delhi, 1993.
5. Koen Bertels, João M.P. Cardoso, Stamatis Vassiliadis, "Reconfigurable Computing: Architectures and Applications", Springer 2006.
6. Kai Hwang and Zu, "Scalable Parallel Computers Architecture"; McGraw Hill Publishing Ltd., 1997.

VE7001	ADVANCED CMOS ANALOG IC DESIGN	L T P C
		3 0 0 3

OBJECTIVES:

- To provide the fundamental concepts of noise in IC, OTA design, switched-capacitor circuits and data conversion circuits.

UNIT I   NOISE IN INTEGRATED CIRCUITS   9

Statistical Characteristics of Noise, Sources of noise, noise models of IC components, Circuit noise calculations, equivalent input noise generators, effect of feedback on noise performance, noise in CS, CE, CG and cascode amplifiers, noise in differential pair, noise bandwidth.

UNIT II   OTA DESIGN CONSIDERATION   9

Step response, Slewing, OTA variations, CMFB implementation, Input resistance, Output resistance, Output Voltage swing, CMRR, PSRR of two-stage telescopic amplifiers.

UNIT III   BANDGAP REFERENCE CIRCUIT AND SWITCHED CAPACITOR
CIRCUITS   9

Supply Insensitive biasing, Temperature insensitive biasing, Sampling Switches, Speed Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers, Switched- Capacitor Integrator, Switched-Capacitor Common-Mode Feedback.

UNIT IV   PERFORMANCE METERICS OF DATA CONVERTERS & NYQUIST RATE D/A CONVERTERS   9

Ideal Sampling, Reconstruction, Quantization, Static performance metrics, Dynamic performance metrics, Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs.

UNIT V   ANALOG TO DIGITAL CONVERTERS   9

Single stage amplifier as comparator, resistor-based latched comparators. offset cancellation, Flash ADC, Successive approximation ADC, Pipelined ADC, Time Interleaved ADC.

TOTAL: 45 PERIODS

OUTCOMES:
At the completion of the subject, students should:
* Be able to grasp the fundamental concept of noise in IC.
* Be able to study and analyze switched-capacitor circuits and the issue of non-linearity and mismatch in the circuits.
* Be able to analyze data conversion circuits such as DAC and ADC and their design techniques.

REFERENCES:
1. Gray, Hurst, Lewis, Meyar, "Analysis and Design of Analog Integrated Circuits" Fifth Edition John Wiley, 2009.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Twelfth Reprint, Tata McGraw Hill, 2012.
3. Rudy Van de Plassche, "CMOS Integrated ADC and DACs" 2nd Edition, Springer,2007
4. Phillip E.Allen, DouglasR.Holberg, "CMOS Analog Circuit Design", Third edition, Oxford University Press, 2011.
5. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010.

NE7074	COMPUTATIONAL INTELLIGENCE	L T P C
		3 0 0 3

OBJECTIVES:
* To provide the basic concepts in computational intelligence.
* To give an exposure to neural network learning techniques and architectures.
* To provide a good understanding of fuzzy concepts and models.
* To provide an exposure to different optimization techniques.

UNIT I   INTRODUCTION TO COMPUTATIONAL INTELLIGENCE   9

Evolution of Computing - Constituents - From Conventional AI to Computational Intelligence - Machine Learning Basics

UNIT II   NEURAL NETWORKS   9

Biological Neurons Networks – Artificial Neural Networks - Supervised -.unsupervised learning - Reinforcement Learning – Activation functions - Perceptrons - Back Propagation networks – Radial Basis Function Networks - Adaptive Resonance architectures - Advances in Neural networks –SVM

UNIT III   FUZZY LOGIC   9

Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions -Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making- Introduction to Fuzzy models

UNIT IV NEURO-FUZZY MODELING 9

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling - Classification and Regression Trees – Data Clustering Algorithms – Neuro-Fuzzy Control - Hybrid learning algorithms - Applications of Neuro-fuzzy concepts

UNIT V OPTIMIZATION ALGORITHMS 9

Heuristic search and optimization techniques – Random search- Introduction to Genetic Algorithms (GA) -Applications of GA – Social Algorithms.

TOTAL = 45 PERIODS

OUTCOMES:

* To be able to design systems based on neural network architectures.
* To implement fuzzy models and work on the fuzzy tool box.
* To design a suitable optimization algorithm for a given application

REFERENCES:

1. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, "Neuro-Fuzzy and Soft Computing", Prentice-Hall of India, 2003.
2. George J. Klir and Bo Yuan, "Fuzzy Sets and Fuzzy Logic-Theory and Applications", Prentice Hall, 1995.
3. James A. Freeman and David M. Skapura, "Neural Networks Algorithms,Applications, and Programming Techniques", Pearson Edn., 2003.
4. Mitchell Melanie, "An Introduction to Genetic Algorithm", Prentice Hall, 1998.
5. David E. Goldberg, "Genetic Algorithms in Search, Optimization and Machine Learning", Addison Wesley, 1997.
6. S. N. Sivanandam, S.Sumathi and S. N. Deepa, "Introduction to Fuzzy Logic using MATLAB", Springer, 2007.
7. S.N.Sivanandam · S.N.Deepa, " Introduction to Genetic Algorithms", Springer, 2007.
8. Jacek M. Zurada, "Introduction to Artificial Neural Systems", PWS Publishers, 1992.

AP7073   DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS   L T P C
                                                            3 0 0 3

OBJECTIVES:

* To discuss the algorithmic complexity parameters and the basic algorithmic design techniques.
* To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms and NP Hard Problems.

UNIT I INTRODUCTION 9

Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II DESIGN TECHNIQUES 9

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III SEARCHING AND SORTING 9

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

UNIT IV   GRAPH ALGORITHMS   9

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms,max-flow min cut theorem, Steiglitz's link deficit algorithm.

UNIT V   SELECTED TOPICS   9

NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

TOTAL: 45 PERIODS

OUTCOMES:
- Will be able to apply the suitable algorithm according to the given optimization problem.
- Ability to modify the algorithms to refine the complexity parameters.

REFERENCES:
1. Sara Baase, "Computer Algorithms : Introduction to Design and Analysis", Addison Wesley, 1988.
2. T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill, 1994.
3. E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia Publications, 1988.
4. D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison
5. Wesley, 1989.

VE7007	DISTRIBUTED EMBEDDED COMPUTING	L T P C
		3 0 0 3

OBJECTIVES:
- To expose the students to the fundamentals of Network communication technologies.
- To teach the fundamentals of Internet
- To study on Java based Networking
- To introduce network routing Agents
- To study the basis for network on-chip technologies

UNIT I   THE HARDWARE INFRASTRUCTURE   9

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.

UNIT II   INTERNET CONCEPTS   9

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

UNIT III   DISTRIBUTED COMPUTING USING JAVA   9

IO streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.

UNIT IV   EMBEDDED AGENT   9

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

UNIT V   EMBEDDED COMPUTING ARCHITECTURE   9

Synthesis of the information technologies of distributed embedded systems – analog/digital co-design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.

TOTAL : 45 PERIODS

OUTCOMES:
At the completion of the course, students will be able to:
- Explain the fundamentals of Network communication technologies, internet, and Java based networking.
- Analyze the analog/digital co-design of distributed embedded computing architecture.

REFERENCES:
1. Dietel & Dietel, "JAVA how to program", Prentice Hall 1999.
2. Sape Mullender, "Distributed Systems", Addison-Wesley, 1993.
3. George Coulouris and Jean Dollimore, "Distributed Systems – concepts and design",Addison –Wesley 1988.
4. "Architecture and Design of Distributed Embedded Systems", edited by Bernd Kleinjohann C-lab, Universitat Paderborn, Germany, Kluwer Academic Publishers, Boston, April 2001, 248 pp.

VE7017	ROBOTICS	L T P C
		3 0 0 3

OBJECTIVES:
- To learn about the dynamics of robotic controls
- To learn about the navigation mechanisms
- To learn about the hardware and software tools required for building robotic systems

UNIT I   INTRODUCTORY ROBOTICS   9
Introduction, Rigid Transformation, Robot anatomy, Kinematics, Inverse Kinematics, Jacobians, Trajectory Following, Statics and Dynamics.

UNIT II   ARTIFICIAL LIFE AND ARTIFICIAL INTELLIGENCE   9
History, Purpose of Robots, Artificial Intelligence, Artificial life- Nano robotics, Using neural neworks in robots, Neural-Behavior based architecture, Fuzzy logic and neural sensors.

UNIT III   HARDWARE TOOLS   9
Microcontrolers, Photovoltaic Cells, Fuel Cells, Batteries.
Movement and Drive Systems- Air muscles, Nitinol wire, Solenoids, Rotary solenoids, Stepper motors, Servo Motors and DC motors.
Sensors-Signal conditioning, Light sensors, Machine vision, Body sense, Direction-magnetic fields, Speech recognition, Sound and ultrasonics, Touch and Pressure, Piezoelectric material, Switches, Bend sensors, Pressure sensor, Smell, Humidity, Testing sensor.
Casestudy: Speech-controlled mobile robot, Behavioral-based robotics, neural networks, nevous nets and subsumption architecture.

UNIT IV   BASIC NAVIGATION   9
Philosophies, Live Reckoning, The Best Laid Plans of Mice and Machines, Navigation as a filtering process, Hard navigation vs Fuzzy navigation, Sensors, Navigation Agents and Arbitration, Instilling pain, Fear and Confidence, Becoming unstuck in Time, Programming Robots to be useful, Command, Control and Monitoring, The Law of Conservation of Defects and the Art of Debugging.

UNIT V   DESIGN OF ROBOTS   9
Telepresence robot, Mobile platforms, Walker Robots, Solar-ball Robot, Underwater bots, Aerobots, Robotic arm and IBM PC interface and speech control, Android hand.

TOTAL:45 PERIODS

OUTCOMES:
Students will be able to
- Build a miniature robotic system
- Explain navigation mechanisms involved in building a robotic system

Attested

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REFERENCES:
1. J. M. Selig, "Introductory Robotics", Prentice Hall, 1992.
2. John Iovine, "Robots, Android and Animatronics", Second Edition, McGraw-Hill, 2002.
3. John M. Holland, "Designing Autonomous Mobile Robots-Inside the mind of an Intelligent Machine", Newnes Publication, 2004.
4. Robert J. Schiling, "Fundamentals of Robotics- Analysis and Control", Pearson Education, 2006.
5. Bruno Siciliano, Lorenzo Sciavicco, Luigi Villani and Giuseppe Oriolo, "Robotics- Modelling, Planning and Control", Springer-Verlag London Limited 2010.

VE7002	ADVANCED EMBEDDED SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES
- To teach the fundamentals on design attributes of functional units of embedded systems.
- To discuss about Hardware, software partitioning in system design
- To introduce architectural features of 32 bit ARM microcontroller.
- To discuss strategies for embedded firmware design and development.
- To develop an integrated development environment in embedded system

UNIT I   TYPICAL EMBEDDED SYSTEM   9
Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Characteristics and Quality Attributes of Embedded Systems: Hardware, Software Co-Design and Program Modeling: Fundamental Issues in Hardware, Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware Software

UNIT II   EMBEDDED HARDWARE DESIGN AND DEVELOPMENT   9
EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port, junction, creating part numbers, Design Rules check, Bill of materials, Netlist creation , PCB Layout Design – Building blocks, Component placement.

UNIT III   ARM -32 BIT MICROCONTROLLER FAMILY   9
Architecture of ARM Cortex M3 –General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. Advanced Programming Features. Memory Protection. Debug Architecture.

UNIT IV   EMBEDDED FIRMWARE DESIGN AND DEVELOPMENT   9
Embedded Firmware Design Approaches, Embedded Firmware Development Languages, Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

UNIT V   EMBEDDED SYSTEM DEVELOPMENT ENVIRONMENT   9
The Integrated Development Environment (IDE), Types of Files Generated on Cross compilation, Disassembler/ELDompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

TOTAL: 45 PERIODS

OUTCOMES:
- Ability to discuss the concepts of typical embedded systems.
- Ability to develop an integrated development environment of hardware/software codesign of embedded system.

Attested

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REFERENCES:
1. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009
2. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier), 2008.
3. James K Peckol, "Embedded Systems – A contemporary Design Tool", John Weily, 2008.

NE7071	ADAPTIVE SIGNAL PROCESSING	L T P C
		3 0 0 3

OBJECTIVES:
- To provide an in-depth coverage of the adaptive filter theory.
- To provide the mathematical framework for the understanding of adaptive statistical signal processing.
- To know the basic tools of vector spaces and discrete-time stochastic process.
- To understand the various issues involved in adaptive filtering.
- Various types of adaptive filters will be introduced and their properties will be studied, specifically convergence, tracking, robustness and computational complexity.
- Learn to apply adaptive filter theory using prescribed case studies.

UNIT I   STOCHASTIC PROCESSES AND SPECTRUM ESTIMATION   9

Statistical characteristics of a stochastic process-Non-Parametric methods - Correlation method - Covariance estimator - Performance analysis of estimators – Unbiased consistent estimators -Periodogram estimator - Barlett spectrum estimation - Welch estimation - Model based approach -AR, MA, ARMA Signal modeling - Parameter estimation using Yule-Walker method.

UNIT II   WIENER FILTERS   9

Optimum Filtering-The normal equations and the Wiener filter-Minimum mean square error estimation and the orthogonality principle- Wiener-Hopf equations- Linear prediction-forward Linear PredictionBackward linear prediction-Levinson-Durbin algorithm.

UNIT III   GRADIENT-BASED ADAPTIVE FILTERS   9

The basic idea of the steepest descent algorithm- The steepest descent algorithm applied to wiener filter – Stability of the steepest descent algorithm- The LMS algorithm-LMS adaptive algorithm-Method of Least Squares-Data windowing-Properties of LS Estimates-MVDR spectrum estimation. Recursive Least Squares (RLS)-Exponentially weighted RLS-Convergence analysis-Sliding window RLS.

UNIT IV   KALMAN FILTERS & TRACKING   9

Statement of the Kalman filtering problem-The innovation process- Estimation– Filtering - Initial conditions. Variants of the Kalman filter-The Extended Kalman filter-Criteria for tracking assessment, Tracking performance of the LMS and RLS algorithms- Comparison.

UNIT V   APPLICATIONS   9

Channel equalization-Echo cancellation- Deconvolution- Adaptive noise cancellation-Adaptive interference cancellation. Case study.

TOTAL: 45 PERIODS

OUTCOMES:
- To be able to solve the problems related to optimal design, convergence, and recursiveness.
- To carry out time/frequency domain implementations of adaptive filters.
- To be able to apply the concepts of stochastic processes to adaptive filters.
- To be able to design adaptive filter algorithms.
- To be able to apply adaptive filter theory to applications such as echo cancelation, noise cancellation and channel equalization.

Attested

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REFERENCES:
1. Simon Haykin, "Adaptive Filter Theory", Pearson Education, Fourth Edition, 2003.
2. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", Wiley, 2008.
3. Ali.H.Sayed, "Fundamentals of Adaptive Filtering", John Wiley & Sons, 2003.
4. Paulo S. R. Diniz, "Adaptive Filtering Algorithms and Practical Implementation", Springer, 2011.
5. Lino Garcia, "Adaptive Filtering Applications", InTech, Published, 2011.
6. Kong-Aik Lee, Woon-Seng Gan, Sen M. Kuo, "Subband Adaptive Filtering: Theory and Implementation", Wiley, 2009.

VE7014	NETWORK ON CHIP DESIGN	L T P C
		3 0 0 3

OBJECTIVES:
- To impart knowledge in the concept of a peer to peer interconnection network, shared bus based design, and network on chip (NoC) based architectures.
- To address the issues of scalability of onchip connectivity and inter processor communication.

UNIT I   INTRODUCTION TO INTERCONNECTION NETWORKS   9
Uses of Interconnection Networks, Network Basics, A Simple Interconnection Network, Network Specifications and Constraints, Topology, Routing, Flow Control, Router Design, Performance Analysis.

UNIT II   TYPES OF NETWORKS   9
Butterfly Networks, Torus Networks Mesh Networks,Non-blocking networks, Non-interfacing networks, Crossbar networks Clos Netwokrs, Beneˇs Networks, Sorting Networks

UNIT III   ROUTING & FLOW CONTROL   9
Routing Basics, Deterministic Routing, Dimension-Order Routing, Adaptive Routing, Adaptive Routing Basics, Minimal Adaptive Routing, Fully Adaptive Routing, Flow control basics, Butterflow control, Buffer Management and Back pressure, A flit reservation flow control, Deadlock and livelock avoidances, Deadlock and livelock avoidances in adaptive routing

UNIT IV   QUALITY OF SERVICE & ROUTER   9
Guranteed services, Best-Effort services, Router Datapath Components, Input Buffer organization, Switches, Output Organization, Arbitration, waveform allocator, Processor-Network Interface, Shared-Memory Interface.

UNIT V   PERFORMANCE ANALYSIS   9
Throughput, Latency, Fault Tolerance, Common Measurement Pitfalls Queuing Theory, Probabilistic Analysis, Application-Driven Workloads, Synthetic Workloads, Virtual Channels, Network Size, Injection Processes, Prioritization, Stability, Fault tolerance.

TOTAL: 45 PERIODS

OUTCOMES:
At the completion of this subject, students should be able to:
- Design and analyze NOC architectures with interconnection networks, routing, shared memory interface, Processor-Network Interface.

REFERENCES:
1. William James Dally and Brian Patrick Towles, "Principles and Practices of Interconnection Networks",The Morgan Kaufmann Series in Computer Architecture and Design,2004.
2. Sudeep Pasricha and Nikil Dutt, On-Chip Communication Architectures - System on Chip Interconnect, Elsevier, 2008.
3. Jih-Sheng Shen and Pao-Ann Hsiung, "Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication" IGI global, Copyright © 2010.

VE7009   **EMBEDDED C**   **L T P C**
                                                                                         3 0 0 3
OBJECTIVES:
- To understand the basics of embedded C programming and its compilers and simulators.
- Apply to C programming in embedded systems.

UNIT I   BASICS OF EMBEDDED C   9
System programmimg Vs Application Programming-General rules in C, Comments, White Spaces, Modules, Data type, Procedures, Variables, Expression and Statements, Structures and Union, Data structures, Program Description Language.

UNIT II   PROGRAMMING   9
Adding Structure to the Code Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Examples.

UNIT III   COMPLIERS AND SIMULATORS   9
Introduction to MikroC compiler and debugger, Functions and Inbuilt libraries in MikroC, Creating new libraries, Development Tools, Introduction to simulators such as Proteus and Real PIC.

UNIT IV   EMBEDDED MEMORY   9
Mixing Assembly and C, Memory Alignment with Structures, Memory management in C, Memory-map of Applications.

UNIT V   CASE STUDIES   9
Chasing LEDs, LED Dice, Seven Segment LED Counter, Two-Digit Muliplexed Seven Segment LED Counter with Timer Interrupt, Real Time Clock, Digital Voltmeter with LCD, Calculator with Keypad and LCD, Serial Communication Based Calculator, Multitasking and Real-Time Operating Systems.

                                                                         TOTAL : 45 PERIODS
OUTCOMES:
- This subject enables our students to create, develop, apply, and disseminate the programming knowledge within the embedded systems development environment.

REFERENCES:
1. Micheal Barr, "Embedded C Coding Standard", Barr Group Publishing, 2013.
2. Milan Verle, "PIC Microcontrollers with Examples in Assembly Language", mikroElektronika Publications, 2008.
3. Milan Verle, "PIC Microcontrollers- Programming in C", mikroElektronika Publications, 2009.
4. Dogan Ibrahim, " Advanced PIC Microcontoller Projects in C- From USB to RTOS with the PIC 18F Series", Newnes Publications, 2008.
5. Mohammad Ali Mazidi, Rolin D. Mckinlay and Danny Causey, "PIC Microcontroller and Embedded Systems using Assembly and C for PIC 18", Pearson India, 2008.

VE7003   **ALGORITHMS FOR VLSI DESIGN AUTOMATION**   **L T P C**
                                                                       3 0 0 3
OBJECTIVES:
- To discuss the algorithms for logic synthesis, verification.
- To discuss about the design tradeoff in various partitioning algorithms, placement, floor planning and pin assignment of VLSI design automation.
- To analyze the different global routing algorithms and compaction in design automation.

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UNIT I   LOGIC SYNTHESIS & VERIFICATION: 6

Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

UNIT II   PARTITIONING: 9

Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

UNIT III   PLACEMENT, FLOOR PLANNING & PIN ASSIGNMENT: 9

Problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

UNIT IV   GLOBAL ROUTING: 12

Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization.

UNIT V   COMPACTION: 9

Problem formulation, one-dimensional compaction, two dimensions based compaction, hierarchical compaction.

TOTAL: 45 PERIODS

OUTCOMES:

Ability to analyze the algorithms needed for synthesis, partitioning, placement, floor planning, routing in VLSI design automation

REFERENCES:

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.
2. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
3. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition 4. Trimburger, "Introduction to CAD for VLSI", Kluwer Academic publisher, 2002
4. Sabih H.Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2007

VE7008	EMBEDDED AUTOMOTIVE SYSTEMS	L T P C
		3 0 0 3

OBJECTIVES

- To teach the Fundamentals of Electronic Components related to automotive applications.
- To discuss on Automotive Sensors, Actuators and Instumentations
- To teach the Control Mechanisms in an Automotive System
- To discuss on Telematics and Diagnostic methods

UNIT I   SYSTEMS APPROACH TO CONTROL AND INSTRUMENTATION   9

System, Linear system theory, Steady-State sinusoidal frequency response of a system, State variable formulation of models, Control theory, Stablity of Control System, Closed-Loop Limit-Cycle Control, Instrumentation, Basic Measurement System, Filtering, Digital Subsystem, Sinusoidal Frequency Response, Discrete Time Control System, Closed loop control, Example Discret Time Control System.

UNIT II FUNDAMENTALS OF ELECTRONICS, MICROCOMPUTER INSTRUMENTATION AND CONTROL 9

Semiconductor Devices, Transistors, ICs, Operational Amplifiers, Use of Feedback in Op Amps, Phase-Locked Loop, Digital Circuits, Logic Circuits (Combination and Sequential Circuits), Timers and Counters, Microcomputer fundamentals, Tasks and Operations, CPU Registers, Reading Instructions, Programming Languages, Microcomputer Hardware, Microcomputer Applications in Automotive Systems, Instrumentation Applications of Mirocomputers, Microcomputers in Control Systems.

UNIT III SENSORS, ACTUATORS AND ELECTRONIC ENGINE CONTROL 9

Motivation for Electronic Engine Control, Exhaust Emissions, Fuel Economy, Test Procedures, Concept of an Electronic Engine Control System, Engine Performance Terms, Exhaust Catalytic Convertors, Electronic Fuel-Control System, Analysis of Intake Manifold Pressure, Idle Speed Control, Electronic Ignition, Automotive Control System Applications of Sensors and Actuators, Throttle Angle Sensor, Temperature Sensor, Coolant Sensor, Sensors for Feed back control, Knock Sensors, Automotive Engine Control Actuators, Variable Valve Timing, Electric Motor Actuators, Ignition System.

UNIT IV MOTION AND DIGITAL POWERTRAIN CONTROL SYSTEM 9

Digital Engine Control, Features, Control Modes for Fuel COntrol, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Electronic Ignition Control, Integrated Engine Control System, Summary of Control Modes, Cruise Control System, Cruise Control Electronics, Antilocking Braking System, Electronic Suspension System, Electronic Steering Control, Four-Wheel Steering.

UNIT V AUTOMOTIVE INSTRUMENTATION, TELEMATICS AND ITS DIAGNOSTICS 9

Modern Automotive Instrumention, Input and Output Signal Generation, Advantages of Computer Based Instrumentation, Display Devices, Flat Panel Display, Fuel Quantity Mesurement, Coolant Temperature Measurement, Oil Pressure Measurement, Vechicle Speed Measurement, High-Speed Digital Communication (CAN BUS), Telematics, GPS Navigation, GPS System Structure, Automotive Diagnostics.

TOTAL : 45 PERIODS

OUTCOMES:
At the successful completion of this courset, students will be able to:
* Discuss embedded controls and mechanisms involved in an automotive systems

REFERENCES:
1. William B. Ribbens, "Understanding Automotive Electronics- An Engineering Prespective", 7th Edition, Butterworth-Heinemann Publications, 2012.
2. Young A.P. & Griffiths, " Automotive Electrical Equipment" , ELBS & New Press,1999.
3. Tom Weather Jr. & Cland c. Ilunter, " Automotive computers and control system", Prentice Hall Inc., New Jersey.
4. Crouse W.H., " Automobile Electrical Equipment" , Mc Graw Hill Co. Inc., New York ,1995.
5. Bechhold, " Understanding Automotive Electronic", SAE,1998.
6. Robert Bosch," Automotive Hand Book", SAE (5TH Edition),2000.

VE7004	COMPUTER AIDED DESIGN FOR VLSI CIRCUITS	L T P C
		3 0 0 3

OBJECTIVES:
* To discuss the Algorithmic Graph Theory and computational complexity optimization.
* To discuss the concepts of layout design rules and floor planning.
* To simulate and synthesis different hardware models.

UNIT I   VLSI DESIGN METHODOLOGIES   9
Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II   DESIGN RULES   9
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning.

UNIT III   FLOOR PLANNING   9
Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV   SIMULATION   9
Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V   MODELLING AND SYNTHESIS   9
High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

                                                                    TOTAL : 45 PERIODS

OUTCOMES:
At the completion of this subject,
- Students will be able to implement, simulate and synthesis the computer aided design of VLSI systems.

REFERENCES:
1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

VE7005	DESIGN OF EMBEDDED CONTROL SYSTEM	L T P C
		3 0 0 3

OBJECTIVES:
- To expose the students to the fundamentals of Embedded System Blocks
- To teach the fundamental RTOS.
- To study on interfacing for processor communication
- To compare types and Functionalities in commercial software tools
- To discuss the Applications development using interfacing

UNIT I   EMBEDDED SYSTEM ORGANIZATION   9
Embedded computing, Characteristics of embedded computing applications, Embedded system design challenges, Build process of Realtime Embedded system, Selection of processor, Memory, I/O devices, Rs-485, MODEM, Bus Communication system using I2C, CAN, USB buses, 8 bit – ISA, EISA bus.

UNIT II   REAL-TIME OPERATING SYSTEM   9
Introduction to RTOS, RTOS- Inter Process communication, Interrupt driven Input and Output, Nonmaskable interrupt, Software interrupt, Thread – Single, Multithread concept, Multitasking Semaphores.

UNIT III INTERFACE WITH COMMUNICATION PROTOCOL 9

Design methodologies and tools – Design flows – Designing hardware and software Interface, System Integration; SPI, High speed data acquisition and interface, SPI read/write protocol, RTC interfacing and programming.

UNIT IV DESIGN OF SOFTWARE FOR EMBEDDED CONTROL 9

Software abstraction using Mealy-Moore FSM controller, Layered software development, Basic concepts of developing device driver, SCI, Software, Interfacing & porting using standard C & C++, Functional and performance Debugging with benchmarking Real-time system software, Survey on basics of contemporary RTOS- VXWorks, UC/OS-II.

UNIT V CASE STUDIES WITH EMBEDDED CONTROLLER 9

Programmable interface with A/D & D/A interface, Digital voltmeter, Control- Robot system, PWM motor speed controller, Serial communication interface.

TOTAL : 45 PERIODS

OUTCOMES:
- Students will be able to realize a real time embedded system.

REFERENCES:
1. Steven F. Barrett, Daniel J. Pack, "Embedded Systems – Design and Applications with the 68HC 12 and HCS12", Pearson Education, 2008.
2. Raj Kamal, "Embedded Systems- Architecture, Programming and Design" Tata McGraw Hill, 2006.
3. Chattopadhyay, "Embedded System Design",PHI Learning, 2011.
4. Steven F.Barrett,Daniel J.Pack,"Embedded Systems-Design & Application with the 68HC12 & HCS12", Pearson Education,2008.
5. Daniel W. Lewis, "Fundamentals of Embedded Software", Prentice Hall India, 2004.
6. Marian Andrzej Adamski, Andrei Karatkevich and Marek Wegrzyn, " Design of Embedded control systems" Springer Science + Busciness Media, 2005.

VE7012 MULTICORE ARCHITECTURES AND PROGRAMMING L T P C
3 0 0 3

OBJECTIVES:
- To discuss the principles of different multiprocessors with their performance issues.
- To discuss the fundamentals of various programming concepts used in multicore architectures.

UNIT I INTRODUCTION TO MULTIPROCESSORS AND SCALABILITY ISSUES 9

Scalable design principles – Principles of processor design – Instruction Level Parallelism, Thread level parallelism. Parallel computer models –- Symmetric and distributed shared memory architectures – Performance Issues – Multi-core Architectures - Software and hardware multithreading – SMT and CMP architectures – Design issues – Case studies – Intel Multi-core architecture – SUN CMP architecture.

UNIT II PARALLEL PROGRAMMING 9

Fundamental concepts – Designing for threads – scheduling - Threading and parallel programming constructs – Synchronization – Critical sections – Deadlock. Threading APIs.

UNIT III OPENMP PROGRAMMING 9

OpenMP – Threading a loop – Thread overheads – Performance issues – Library functions. Solutions to parallel programming problems – Data races, deadlocks and livelocks – Non-blocking algorithms – Memory and cache related issues.

UNIT IV   MPI PROGRAMMING   9

MPI Model – collective communication – data decomposition – communicators and topologies – point-to-point communication – MPI Library.

UNIT V   MULTICORE ARCHITECTURES FOR EMBEDDED SYSYETMS   9

Architectural Considerations, Interconnection Networks, Software Optimizations.
Case Studies: HiBRID SoC for Multimedia Signal Processing, VIPER Multiprocesssor SoC, General Purpose Multiprocessor DSP, Multicore DSP Platforms.

TOTAL : 45 PERIODS

OUTCOMES:
- Students will be able to explain the principle and operation of multicore architectures and their programming.
- Students will be able to design a multicore architecture for an embedded system.

REFERENCES:
1. Shameem Akhter and Jason Roberts, "Multi-core Programming", Intel Press, 2006.
2. Michael J Quinn, Parallel programming in C with MPI and OpenMP, Tata Mcgraw Hill, 2003.
3. Georgios Kornaros, "Multicore Embedded systems", CRC Press, Taylor & Francis Group, 2010.
4. John L. Hennessey and David A. Patterson, " Computer architecture – A quantitative approach", Morgan Kaufmann/Elsevier Publishers, 4th. edition, 2007.
5. David E. Culler, Jaswinder Pal Singh, "Parallel computing architecture : A hardware/ software approach" , Morgan Kaufmann/Elsevier Publishers, 1999.
6. Bryon Moyer, "Real world Multicore Embedded systems", Elsevier, 2013.
7. Gerassimos Barlas, "Multicore and GPU Programming: An Integrated Approach", Elsevier, 2015.

VE7010   **EMBEDDED NETWORKING**   **L T P C**
                                                                          3 0 0 3

OBJECTIVES:
To impart knowledge on
- Serial and parallel communication protocols
- Application Development using USB and CAN bus for PIC microcontrollers
- Application development using Embedded Ethernet.
- Wireless sensor network communication protocols.

UNIT I   COMMUNICATION PROTOCOLS: 9

Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT II   USB AND CAN BUS: 9

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC Microcontroller USB Interface – CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT III   ETHERNET BASICS: 9

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT IV   EMBEDDED ETHERNET: 9
Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT V   WIRELESS EMBEDDED NETWORKING: 9
Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TOTAL : 45 PERIODS

OUTCOMES:
- Complete knowledge of wired and wireless network protocols
- Should be able to incorporate networks in embedded systems

REFERENCES:
1. Frank Vahid, Tony Givargis, "Embedded Systems Design: A Unified Hardware/Software Introduction" - John & Wiley Publications, 2002
2. Jan Axelson, "Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port" - Penram Publications, 1996.
3. Dogan Ibrahim, "Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series" - Elsevier 2008.
4. Jan Axelson, "Embedded Ethernet and Internet Complete", Penram publications, 2003.
5. Bhaskar Krishnamachari, Networking, Wireless Sensors - Cambridge press 2005.
6. Olaf Pfeiffer, Andrew Ayre and Christian Keydel, "Embedded Networking with CAN and CANopen", Second edition published by Copperhill Media Corporation, 2003.

| NE7076 | DIGITAL IMAGE AND VIDEO PROCESSING | L T P C |
| | | 3 0 0 3 |

OBJECTIVES:
- To provide the basic concepts of image & pattern recognition.
- To give an exposure to basic image processing and modeling techniques.
- To provide an understanding of various concepts related to video object extraction.
- To prepare students for development and implementation of algorithms

UNIT I   IMAGE FUNDAMENTALS AND TRANSFORMS   9
Image Representation- Sampling and Quantization - Two dimensional DFT- Discrete cosine Transform - Walsh - Hadamard transform - Wavelet transform - Construction of Wavelets-Types of wavelets - principal component analysis.

UNIT II   PROCESSING AND MODELING OF IMAGES   9
Pre-processing -Point operations – contrast stretching – Histogram - Histogram equalization - Image segmentation- pixel based, edge based, region based segmentation - Morphological image processing - Edge and texture models - Image registration - Colour Image Processing -

UNIT III   SPATIAL FEATURE EXTRACTION   9
Feature selection - Localized feature extraction- Boundary Descriptors - Moments - Texture Descriptors - Co-occurrence features

UNIT IV   CLASSIFIERS   9
Kernel based approaches - clustering methods - Maximum Likelihood Estimation- Bayesian approach- Pattern Classification

Attested

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UNIT V   VIDEO OBJECT EXTRACTION   9
Back ground subtraction – Frame difference - Static and dynamic background modeling - optical flow techniques-Handling occlusion- scale and appearance changes - Shadow removal.

TOTAL :45 PERIODS

OUTCOMES:
* To be able to design pattern recognition systems.
* To design and implement feature extraction techniques for a given application.
* To design a suitable classifier for a given application.

REFERENCES:
1. A.K.Jain, "Fundamentals of Digital Image Processing", Prentice-Hall, 2002.
2. R.C.Gonzalez and R.E.Woods, 'Digital Image Processing', Second Edition, Pearson Education, 2002.
3. A.Bovik, "Handbook of Image and Video Processing", 2nd Edition, Academic Press, 2005.
4. Mark Nixon and Alberto Aguado, "Feature Extraction and Image Processing", Academic Press, 2008.
5. John C.Russ, "The Image Processing Handbook", CRC Press, 2007.
6. Richard O. Duda, Peter E. Hart and David G. Stork., "Pattern classification", Wiley, 2001

VE7006	DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES	L T P C
		3 0 0 3

OBJECTIVES:
* To understand the architecture and programming of fixed and floating point DSP processors.
* To understand the techniques involved in real time DSP system design and to design and implement a variety of DSP algorithms for real world applications.
* To gain the practical knowledge of real time implementation issues.
* Learn the basic forms of FIR and IIR filters, and design filters with desired frequency responses.
* Understand the fast implementation schemes of DFT.
* Learn to apply adaptive filter theory and implement it in DSP Processor.

UNIT I   INTRODUCTION TO DIGITAL SIGNAL PROCESSING SYSTEMS   9
Fundamentals of DSP - Digital signal processor architectures – Software developments – Hardware issues – System considerations – Implementation considerations, Data representations, Finite word length effects, Programming issues, Real time implementation considerations.

UNIT II   FIXED AND FLOATING POINT DIGITAL SIGNAL PROCESSORS   9
TMS320C55x – Architecture overview, Addressing modes, Instruction set, Programming considerations, system issues. TMS320C62x AND TMS320C64x - Architecture overview, Memory systems, External memory addressing, Instruction set, Programming considerations, system issues. TMS320C67X – Architecture overview, Instruction set, Pipeline Architecture, Programming considerations, Realtime implementations.

UNIT III   FAST FOURIER TRANSFORMS   9
Introduction to DFT – FFT algorithms – Decimation-in-time, Decimation-in-frequency - Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

UNIT IV   FIR AND IIR FILTER IMPLEMENTATIONS   9
FIR and IIR filters – Characteristics, Structures, FIR Filter design using Windowing and frequency sampling method, IIR Filter-Butterworth and Chebyshev Filter Design-, Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

Attested

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UNIT V   ADAPTIVE FILTER STRUCTURES AND ALGORITHMS   9

Wiener filter, LS filter , Filter structures, Adaptive algorithms, Properties and Applications – Fixed and floating point implementation using TMS320C64x and TMS320C67x.

TOTAL: 45 PERIODS

OUTCOMES:
- To be able to develop the program for fixed and floating point DSP processors based on the design issues.
- To be able to design and develop real time implementations on DSP algorithms.
- Ability to design IIR and FIR filters.
- To apply the fast transforms for the analysis of DSP systems.
- To be able to realize and implement a suitable structure for FIR and IIR Filters.
- To be able to design adaptive filter algorithms.

REFERENCES:
1. Sen M.Kuo, Woon-Seng S.Gan, "Digital Signal Processors – Architectures, Implementations and Applications", Pearson Education, 2005, Second Impression, 2009.
2. Lapsley et al "DSP Processor Fundamentals, Architectures & Features" S.Chand & Co, 2000, Reprint.
3. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", Wiley, 2008.
4. John G Proakis and Manolakis, "Digital Signal Processing Principles, Algorithms and Applications", Pearson, Fourth Edition, 2007.
5. TMS Manual on TMS320C64XX and TMS320C67XX.
6. A.V. Oppenheim, R.W.Schafer and J.R.Buck, "Discrete Time Signal Processing", Pearson, 2004.
7. S.K. Mitra, "Digital Signal Processing, A Computer Based approach", Tata McGraw-Hill, 1998.
8. P.P. Vaidyanathan, "Multirate Systems & Filter Banks", Prentice Hall, 1993.
9. I.C.Ifeachor and B.W. Jervis, "Digital Signal Processing-A Practical Approach", Pearson, 2002.

Attested

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